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Extended Linear Phase Detector Characteristic of a Software PLL

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***Abstract*—Synchronization is a critical operation in digital communications. An important part of the synchronizer structures relies on the digital phase locked loop (PLL) principle.**
The PLL structure can be derived from the maximum likelihood (ML) criterion, leading to a sinusoidal phase error detector (PED). This PED offers robustness at low signal-to-noise ratio (SNR) transmissions. However, the reduced linear zone of the PED characteristic leads to unwanted cycle slips in the presence of large frequency offset. On the other side, the tanlock PED has an extended linear characteristic but is still limited in the case of simultaneous large frequency offset and low SNR transmissions in both acquisition and tracking modes.
We propose in this paper a software PLL which stays quasi-linear for low SNR and large frequency offset transmissions. Simulations show that the proposed system is robust to cycle slips. Moreover, this system can be designed with the classical tools used for the linear model of the PLL.

I. Introduction

Software PLLs (or all-digital PLLs) are nowadays commonly implemented on digital signal processor (DSP). [1], and more recently [2]–[4] provide a detailed overview on the implementation of software PLL. All-digital PLL may offer significant advantages compared to their analogic counterpart in term of performance and flexibility.
Sinusoidal phase error detectors (PED) have been used extensively in the past in digital PLL implementation. They offer good properties in a noisy environment: the sinusoidal PED is extracted from the maximum likelihood criterion [1]. However, it exhibits poor frequency tracking capabilities in the presence of large frequency offset due to its reduced linearity zone, particularly in the case of low signal-to-noise ratio (SNR).
Changing the loop filter coefficients to improve the tracking range of the PLL will result in extending the noise equivalent bandwidth [3]–[5], resulting simultaneously in a better acquisition time and an extended tracking range but also causing a degradation on the variance of the carrier phase estimation.
A smart approach to overcome the trade-off between the acquisition time and the variance of the carrier phase estimation is to use an adaptive algorithm that jointly optimizes the phase estimation and the loop filter parameters [6]. This solution will not be detailed further in this paper but we can note that this algorithm already assumes a linear PED.
Extending the linear zone of the PED characteristic (also denoted S-Curve in the literature) results in extending the tracking range of the PLL without altering the precision of the carrier phase estimation. Compared to the sinusoidal PED, the tanlock PED characteristic has an extended linear zone [5], [7]. The digital tanlock PED is proposed in [7] for a non-uniform sampling PLL.
In [3] it is proposed to extend further the tanlock loop via an unwrapping of the phase error signal (tanlock-unwrapping PED). This system enables the loop to face potentially an infinite range of residual frequency for high SNR transmissions. No further details are given in [3] about the acquisition performance of the PLL implemented with the tanlock-unwrapping PED. However, simulations show that it exhibits poor performance in a low SNR context due to the non-linearity introduced by the unwrapping system.
The contribution of this paper is to propose an additive filtering device to the unwrapping system proposed in [3], which produces a quasi-linear system even for low SNR transmissions. Simulations show that this PLL is particularly robust to simultaneously large frequency offset and low SNR transmissions. The system can be designed with the classical tools used for the linearized PLL. Finally, the quasi-linearity of the system provides high robustness to cycle slips.
The paper is organized as follow: in section II we present the PLL used in the practical case of carrier recovery for digital transmissions. Then, we present in section III the linear model of the software PLL and the main tools to design the digital loop filter. In section IV we compare the sinusoidal and the tanlock loop performance to the linear model of the PLL. Section V of this paper gives details on the innovation and finally section VI concludes.

II. The PLL in a Digital Transmission Context

We consider a QPSK modulated data signal received with an unknown phase and corrupted by an additive white gaussian noise (AWGN) introduced by the channel. We assume in this study perfect symbol timing synchronization and no inter-symbol interference (ISI). Under these assumptions, the received and sampled signal from the input channel can be written as:

$$r_\theta[k] = r_\theta(kT) = \sqrt{2P}\,\Re\left\{d_k\, e^{j(\omega_0 kT+\theta[k])}\right\} + N[k],$$

where ω_0 is the carrier pulsation supposed to be known at the receiver and $\theta[k]$ the unknown carrier phase. $\Re\{u\}$ denotes the real part of the complex u, P the carrier signal power

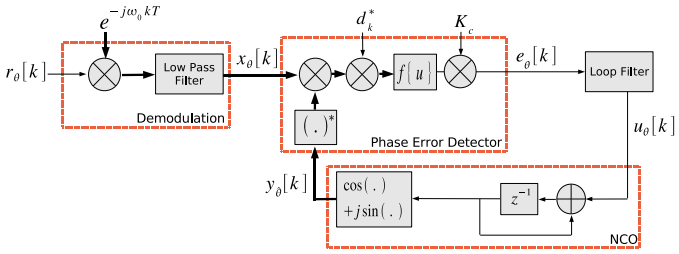

Fig. 1. Block diagram of a digital data-aided carrier demodulator

and $N[k]$ the additive noise signal, supposed to be white and gaussian, with variance σ^2. The input SNR is expressed as P/σ^2. d_k is a QPSK data symbol transmitted at time kT where T is the known symbol period. We consider the particular case of data-aided feedback algorithm derived from the maximum likelihood criterion (DAMLFB). The phase of the received carrier is equal to:

$$\theta[k] = \omega_d kT + \Theta_0, \tag{1}$$

where $\omega_d = 2\pi f_d$ and f_d is the frequency offset (also known as the phase ramp), due to a residual carrier offset and/or a supposed constant Doppler shift. Θ_0 is the phase step, which can be considered as a random variable with a uniform distribution on $[-\pi, \pi]$. Fig.1 depicts a baseband carrier phase demodulator using the DAMLFB criterion classically used in a all-digital receiver, in particular in low SNR transmission context where the use of pilot symbols is particularly relevant. The single frequency sinusoid is transposed into a complex baseband signal by means of a multiplication with a complex exponential running at the carrier frequency. Assuming perfect low pass filters at the demodulation part, the demodulated signal can be expressed in its complex envelope as:

$$x_\theta[k] = \frac{A}{2} d_k \, e^{j\theta[k]} + W[k]. \tag{2}$$

where $W[k]$ is the noise component. The output signal from the numerically controlled oscillator (NCO) is given by

$$y_{\hat{\theta}[k]} = e^{j\hat{\theta}[k]}, \tag{3}$$

where $\hat{\theta}[k]$ is the phase output from the NCO at time $t = kT$. The PED is characterized by the function $f\{u\}$: $f\{u\} = \Im\{u\}$ for the sinusoidal PED, where $\Im\{u\}$ denotes the imaginary part of the complex u and $f\{u\} = \text{Arg}\{u\}$ for the tanlock PED, where $\text{Arg}\{u\}$ denotes the argument of the complex u. At the PED output the phase error signal is expressed as:

$$e_\theta[k] = K_c \, f\left\{x_\theta[k] d_k^* e^{-j\hat{\theta}[k]}\right\}, \tag{4}$$

where K_c is the phase detector gain and * denotes the complex conjugate operator. For both PEDs, this result in a non-linear feedback control system, leading to a non-straightforward analysis.

The loop filter, characterized by the transfer function $Q(z)$, filters the phase detector output and controls the nature of the loop response [1]. Several loop filters are proposed in [1], but the most commonly used is the proportional plus integrator (PI) loop filter, which has the property to have no steady state phase error in the presence of a frequency offset on the received carrier phase:

$$Q(z) = K_1 + K_2 \frac{z}{z-1}, \tag{5}$$

where K_1 and K_2 are the two loop filter parameters that control the stability and are designed to offer the best trade-off between the signal error variance and the acquisition time of the PLL [4].

The numerical controlled oscillator is the digital counter part of the voltage controlled oscillator used in the classical analog PLL. It comprises an integrator and a digital modulator that uses sine and cosine look up tables (Fig.1).

III. Linear Model and Loop Filter Design

The block diagram of the linear model is given in Fig.2. The linearized model of the PLL is obtained by replacing the incoming and the corrected signal by their phases. The local oscillator is removed, keeping only the integrator of the NCO. Thus, only operations made on the phase are kept in the loop. We note:

$$\Delta_\theta[k] = \theta[k] - \hat{\theta}[k] + W_\theta[k], \tag{6}$$

where $W_\theta[k]$ is a noise component. Assuming $K_c = 1$, when the approximation:

$$e_\theta[k] \approx \Delta_\theta[k]$$

is true, the PLL is said to be in lock and the linear model of the PLL is considered as valid. The PLL can then be considered as a digital filter. Noting $h[k]$ the impulse response of the digital filter, $\hat{\theta}[k]$ can be expressed as:

$$\hat{\theta}[k] = (\theta * h)[k], \tag{7}$$

where $*$ denotes the convolution operation. The impulse response $h[k]$ can be expressed in the Z domain:

$$H(z) = \frac{K_1(z-1) + K_2 z}{(z-1)^2 + K_1(z-1) + K_2 z} \tag{8}$$

Expressing the transfer function $H(z)$ in term of its poles and zeros, in the particular case of the second-order loop we obtain:

$$H(z) = \alpha \frac{z - z_0}{(z - z_1)(z - z_2)},$$

where z_1 and z_2 are the two poles and z_0 is the zero of the transfer function $H(z)$. It can be also written in the discrete-time domain through straightforward computations using the inverse Z transform:

$$h[k] = \frac{\alpha}{z_1 - z_2}\left[(1 - \frac{z_0}{z_1}) z_1^k - (1 - \frac{z_0}{z_2}) z_2^k\right], \; k \geq 1 \tag{9}$$

Assuming that the poles are complex, the filter response will be underdamped [2]. The condition:

$$|z_1| = |z_2| < 1 \tag{10}$$

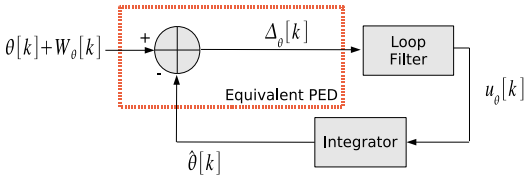

Fig. 2. Block diagram of the linear model

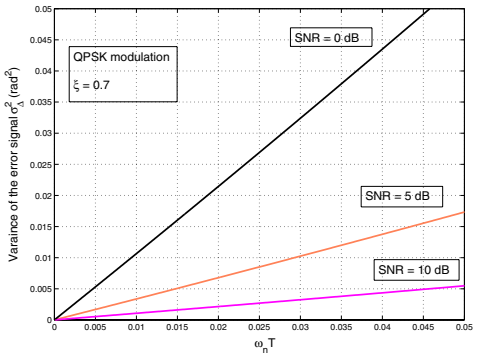

Fig. 3. Plot of the phase error variance σ^2_Δ function of $\omega_n T$

ensures the stability of the PLL.
The poles and the zeros of the filter can be expressed by more appropriate variables than the loop filter parameters:

$$z_1 = z_2^* \quad = \quad 1 - \omega_n T\xi + j\omega_n T\sqrt{1-\xi^2},$$

where ξ and $\omega_n T$ are expressed in terms of K_1 and K_2 as:

$$\begin{aligned} \xi &= \frac{1}{2}\frac{K_1 + K_2}{\sqrt{K_2}}, \\ \omega_n T &= \sqrt{K_2}. \end{aligned}$$

The same results can be found in [2] leading to strictly the same numerical values for ξ and $\omega_n T$.
ξ is called the damping factor and has typically the value $\xi = 1/\sqrt{2}$ [2]. $\omega_n T$ is commonly referred as the normalized natural pulsation of the loop.
It is well known that assuming the linear model of the PLL valid, the signal error variance σ^2_Δ is a linear function of the SNR and the normalized noise equivalent bandwidth $B_L T$ [2], [4]:

$$\sigma^2_\Delta = \frac{B_L T}{SNR}.$$

The normalized noise equivalent bandwidth can be evaluated through straightforward computation, knowing (9) and applying the Parseval's theorem:

$$B_L T = \sum_{l=-\infty}^{+\infty} \left|h[l]\right|^2,$$

we obtain:

$$B_L T = \frac{\alpha^2}{2\Im\{z_1\}}\left[\frac{|z_1 - z_0|^2}{1-|z_1|^2} - \Re\{\frac{(z_1 - z_0)^2}{1 - z_1^2}\}\right].$$

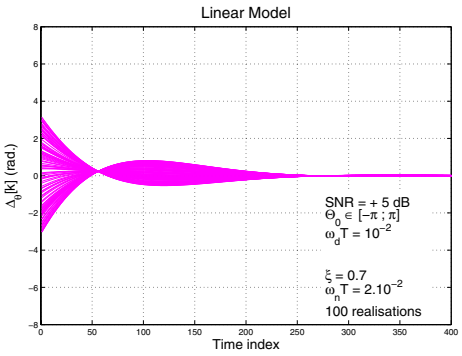

Fig. 4. Phase error signal $\Delta_\theta[k]$, $SNR = +5\,dB$, $\omega_d T = 0.01$.

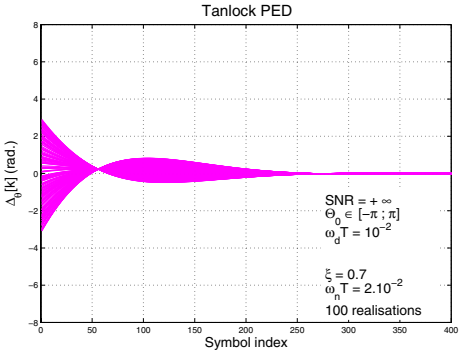

Fig. 5. Phase error signal $\Delta_\theta[k]$, $SNR = +5\,dB$, $\omega_d T = 0.01$.

An another expression of the noise equivalent bandwidth can be found in [2]. We have verified that the two expressions lead to the same numerical values.
Assuming $\xi = 1/\sqrt{2}$ and a constant SNR on the transmission, we plot on Fig.3 the asymptotic phase error variance σ^2_Δ function of the loop filter parameter value $\omega_n T$ for QPSK modulation. For a low SNR transmission (SNR = 0 to 5 dB) context, we observe on Fig.3 that a reliable estimation of the unknown phase $\theta[k]$ could be considered for $\omega_n T = 2.10^{-2}$. The acquisition time of the PLL can be defined as the minimum value of the time index k where the estimation error is close to a stable equilibrium point. At this point, the PLL is said to be in lock. Setting the parameter $\omega_n T$ at a too small value will result in a excessive acquisition time. Implementing the linear model of the PLL we plot on Fig.4 the phase error signal $\Delta_\theta[k]$ and we verify that the acquisition time is acceptable for a data-aided estimation (roughly 150 sample time). Θ_0 is assumed to be a random variable with uniform distribution on $[-\pi; \pi]$, SNR = $5\,dB$ and $\omega_d T = 0.01$.

The acquisition time of the linear model gives a reference compared to the acquisition time of the software PLL.

IV. Comparison of the sinusoidal and the tanlock PED

We implement the software PLL and we compare the results obtained with the sinusoidal and the tanlock PED. For the first simulation, we assume no noise on the transmission (SNR

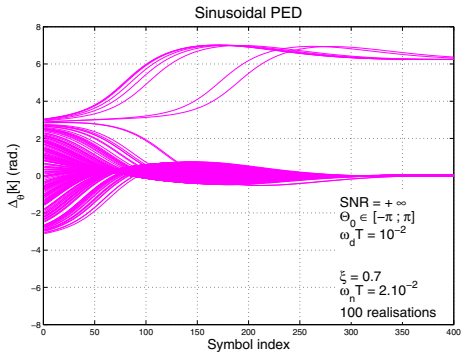

Fig. 6. Phase error signal $\Delta_\theta[k]$, $SNR = +5\,dB$, $\omega_d T = 0.01$.

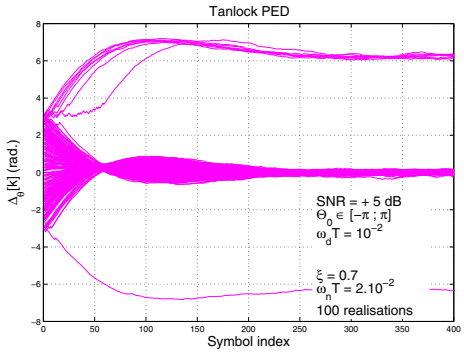

Fig. 7. Phase error signal $\Delta_\theta[k]$, $SNR = +5dB$, $\omega_d T = 0.01$.

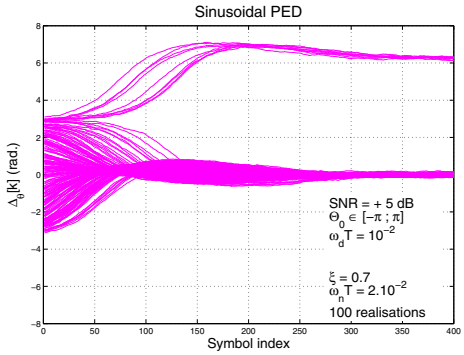

Fig. 8. Phase error signal $\Delta_\theta[k]$, $SNR = +5dB$, $\omega_d T = 0.01$.

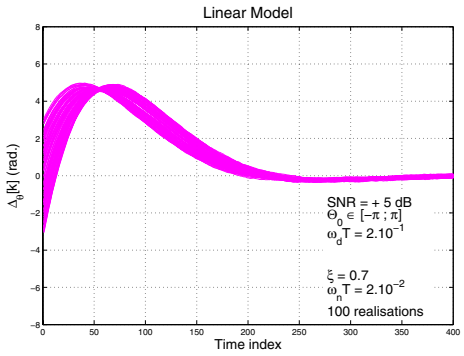

Fig. 9. Phase error signal $\Delta_\theta[k]$, $SNR = +\infty$, $\omega_d T = 0.2$.

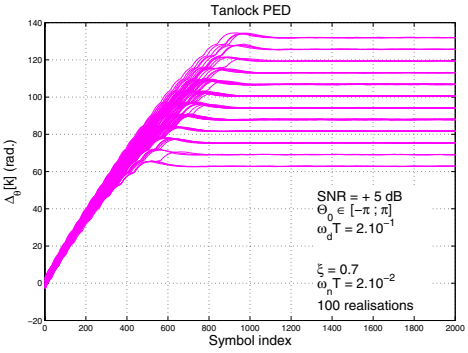

Fig. 10. Phase error signal $\Delta_\theta[k]$, $SNR = 5dB$, $\omega_d T = 0.2$.

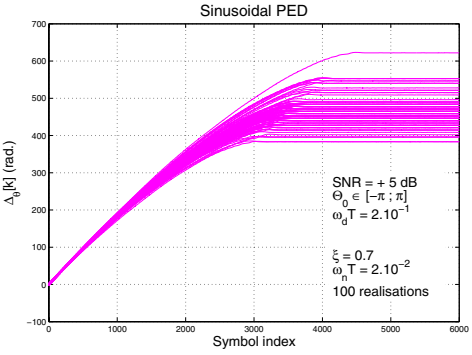

Fig. 11. Phase error signal $\Delta_\theta[k]$, $SNR = 5dB$, $\omega_d T = 0.2$.

$= +\infty$), Θ_0 a random variable with uniform distribution on $[-\pi; \pi]$ and $\omega_d T = 0.01$. We observe on Fig.6 that the results obtained with the tanlock PED are very similar to those obtained with the linear model (Fig.4). On the other hand, for the sinusoidal PED we can observe cycle slip and/or hang-up [9] that cause an impact on the acquisition time, since the sinusoidal PED can no longer be assumed linear when Θ_0 reaches a high value (Fig.5).

Since the phase estimation is correct modulo 2π, the PLL is considered as in lock as soon as the phase error signal $\Delta_\theta[k]$ is nearly equal to 0 modulo 2π. Therefore even in the case of cycle slips, the PLL may still lock in the cost of additional acquisition time.

On a low SNR transmission (SNR = 5 dB), the linear approximation for the tanlock PED becomes also no more valid (Fig.7), but the PLL still locks in a acceptable acquisition time when a cycle slip occurs.

In the case of simultaneous large frequency offset ($\omega_d T = 0.2$) and low SNR transmissions, we observe that the acquisition time of the linear model is still acceptable (Fig.9). However, on Fig.10 and Fig.11 we observe that the PLL keeps on cycle-slipping, resulting in a crippling acquisition time: about $1000\,T$ for the tanlock PED and $4500\,T$ for the sinusoidal PED in the worst case: the linear model of the PLL can not

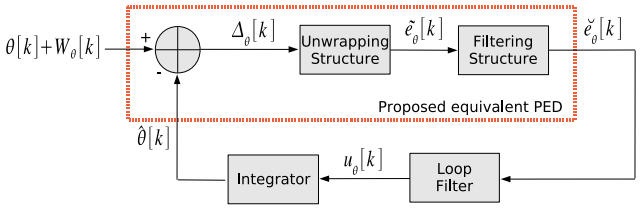

Fig. 12. Block diagram of the equivalent unwrapping loop

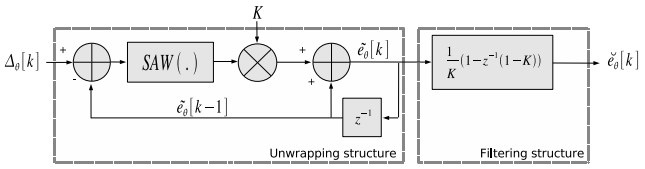

Fig. 13. Proposed equivalent PED

be considered as relevant in the case of large frequency offset transmissions.

V. Proposition of a new phase error detector

We propose a new phase error detector, based on the observation that the non linear behavior of the PLL comes from the overshoot of the phase error signal that goes beyond the linear zone [3]. We propose to add here the unwrapping structure that has been proposed in [8] for an open loop timing recovery scheme, and that we adapt to closed-loop estimation scheme. The block diagram of the system proposed is plotted in Fig.12. More details on the implementation of the unwrapping structure can be found in [8] and [9]. Details of the proposed PED are plotted in Fig.13.
The sawtooth function $SAW(x[k])$ is defined as:

$$SAW(x[k]) = MOD_{2\pi}(x[k] - \pi) - \pi,$$

where $MOD_{2\pi}$ denotes the modulo 2π operation. We observe that when $-\pi \leq x[k] \leq \pi$, $SAW(x[k]) = x[k]$. The unwrapping structure can be considered in this particular case as a filter with transfer function:

$$F_{unw}(z) = \frac{K}{1 - z^{-1}(1-K)}.$$

Observing that the case $-\pi \leq x[k] \leq \pi$ is the general case when the PLL is in lock and that the PED is supposed to be a memoryless function, we propose to cascade the filtering structure $F_{unw}^{-1}(z)$ at the output of the unwrapping structure (denoted on figure Fig.15 as the tanlock unwrapping + filtering PED). Therefore, the proposed PED can be considered as memoryless when the PLL is in lock. The transfer function of the linear model of the PLL can be considered as a relevant estimation.
Simulations show that the tanlock unwrapping PED implemented on the PLL is unable to provide a reliable estimation on low SNR transmissions when $K = 1$, due to the non linearity present in the unwrapping structure (Fig.14). Significant better results can be obtained setting $K < 1$. The unwrapping structure introduces an additional filter when the PLL is in lock, modifying the impulse response of the linear model of the PLL. Moreover the PED characteristic of the PLL comprises an unwanted memory operation. Adding the filtering structure as depicted in Fig.13 restores the linear PED characteristic of the PLL in lock and leads to great improvements on the stability of the estimation. We observe that the system proposed remains robust and approaches well the linear model even for low SNR transmissions (Fig.15).

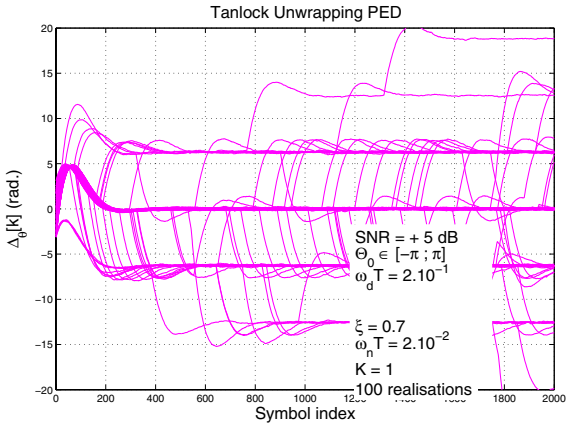

Fig. 14. Phase error signal $\Delta_\theta[k]$, $SNR = 5dB$, $\omega_d T = 0.2$, $K = 1$

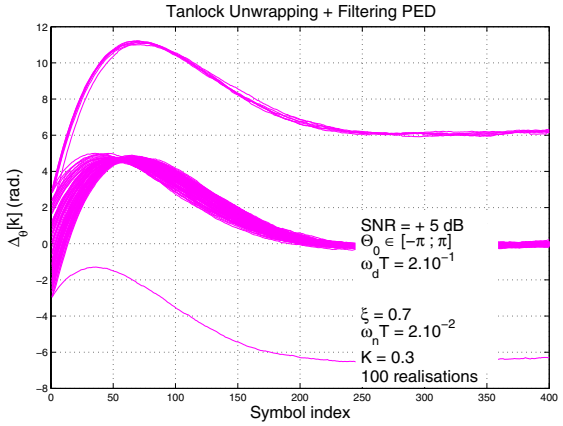

Fig. 15. Phase error signal $\Delta_\theta[k]$, $SNR = 5dB$, $\omega_d T = 0.2$, $K = 0.3$

VI. Conclusion

We have proposed in this paper a software (or all-digital) PLL which stays quasi-linear for low SNR and large frequency offset transmissions. The PLL loop filter has been designed with the help of the linear model of the PLL. The linear model provides a reference on the desired performance of the loop. Simulations have shown that the quasi-linearity of the system proposed introduces high robustness to cycle slips. All these improvements are obtained in the cost of a reduced additional complexity.

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