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Abstract
Further miniaturization of surface electrode ion trap is restricted by wire bonding connection. To resolve this restriction, integration of conventional surface electrode ion trap with through silicon via (TSV) interconnects is proposed and preliminarily demonstrated. Located directly underneath the DC and RF electrodes, TSVs can transmit the electrical signal from interposer to the electrodes on the top. In this work, electrostatic simulation and fabrication processes are introduced to justify the feasibility of this integration. From the electrical characterization (I-V and C-V tests) results, TSV-integrated ion trap exhibits smaller leakage current and lower capacitance than its wire bonding counterparts due to the elimination of large surface area.

Introduction
As compared to conventional quadrupole or liner ion trap [1], surface electrode (SE) ion trap (also known as planar Paul trap) has been reported to exhibit superior scalability, flexibility and compatibility with the state-of-the-art CMOS fabrication technologies. Therefore, SE ion trap is one of promising approaches to realizing large-scale quantum computing. Utilizing the combined electric field induced by co-planar static (DC), radio frequency (RF), and ground (GND) surface electrodes, the charged particle can be confined above the electrode surface, where optical addressing will be exerted for quantum information processing [2].
For further scaling of planar Paul trap, the surface electrodes should be miniaturized with compact trap configurations. However, conventional wire bonding on planar Paul trap occupies a relatively large surface area and disrupts the optical addressing, limiting its miniaturizations [3]. Furthermore, wire bonding is technically challenging in some specific SE configurations, such as ring traps [4, 5]. Thus, to mitigate this issue, we proposed a design that uses TSV to replace wire bonding in electrical signals delivery, providing a fine-pitch I/O path from the interposer on the bottom die to surface electrode on the top die. In addition, the use of interposer can offer SE ion trap with higher functional flexibility without extra surface electrode configuration modification.
Differing from through silicon oxide via [5] and polysilicon filled via [6], a completely CMOS-compatible copper-filled TSV integrating with SE ion trap is introduced in this study. In this work, the trap integrated with TSV is denoted as “TSV trap”. We demonstrated the design, simulation, fabrication and initial electrical characterization of the TSV trap.

Proposed Design and Modeling
One advantage of using TSV in surface electrode ion trap is the scalability, where ~90% of original surface area can be eliminated as compared to its wire bonding counterparts. At the same time, large electric parasitic resistance and inductance induced by long wire bonding will be reduced. Therefore, based on the configuration of planar Paul traps design [7], configuration-modified SE traps with integrated TSVs stacking on silicon interposer are

correspondingly designed as illustrated in Fig. 1. According to different RF electrode width (40 and 80 μm), the planar traps are labeled as V40 and V80, respectively. For V40, two types of TSV traps are developed. The first type with modified geometry is shown in Fig. 1(b) and labeled as REV_V40_TSV. The original wire bonding pads are removed for all DC and RF electrodes and additional small pads are designed for landing TSV arrays on the top die. In the other type (labeled as V40_TSV), the full geometrical dimensions of planar die are maintained. For V80, due to the relatively large RF/DC line width (80 μm), TSVs can be accommodated directly underneath these electrodes. Therefore, all wire-bonding pads and connecting lines are eliminated without adding additional pads. This design is labeled as V80_TSV. The geometry parameters of planar and TSV traps are summarized in Table I. According to analytic solution [8, 9] in typical five-wire electrode configuration [10], the ion trapping height is a factor solely determined by the dimension of the three central electrodes (2 RF, 1 GND). In addition, if the ion specie (88Sr+ in this work), operating amplitude and frequency for RF signal are fixed in ion-trapping operations, the trapping depth can be determined. In other words, these two factors in ion trap have no direct relation with the size or shape of the outer DC/GND electrodes. However, the abovementioned can only be established with the assumptions that the length of center electrodes is infinite and the gaps between them are infinitely small. In actual design and experimental conditions, both assumptions are unachievable. Therefore, it is necessary to perform a numerical simulation to figure out the possible effect of the modification of surface electrode geometry on the ion trapping height and trapping depth.

Three-dimensional models before and after modification are built accordingly. A RF voltage with 200 V amplitude (peak to peak) and 56 MHz is applied on two RF electrodes simultaneously, while other electrodes are set as ground. Based on the obtained electric field above the electrode surface, pseudopotential at the trap point is derived and compared along y-axis (see Fig. 2). The trapping height is the distance from pseudopotential minimum to the electrode surface, while the trapping depth is the pseudopotential difference between saddle point and trap point. From the simulation results, it is postulated that trapping heights (42 μm for V40, and 76 μm for V80) are maintained and changes in trapping depth are negligible.

Fabrication of TSV Trap

The fabrication uses completely CMOS-compatible processes on a 12-inch silicon wafer. TSV is designed with 100 μm height and an aspect ratio of 5. Three geometrical measurements on the TSV opening diameter are performed at the top (16.9 μm), middle (19.1 μm), and bottom (18.2 μm) part of TSV to evaluate its diameter uniformity. After via etching, silicon oxide liner, Ti barrier layer and Cu seed layer are conformally deposited along the TSV pillars. To ensure the TSVs' dielectric strength is sufficiently high, a thick SiO2 liner of 750 nm is used. The morphological features of the TSV opening are showed in Fig. 3. After Cu electroplating, Cu CMP, SiN cap deposition, oxide opening and etching, SiN etching and surface electrode patterning are carried out sequentially at the front side of the top die. Next, a handle wafer is bonded to the front side of the top die, and back side processes including wafer thinning, dielectric pattering and micro bump forming are performed. The fabrication of interposer die is also carried out simultaneously. In the end, top die and interposer die will be bonded together.

Electrical Characterization and Discussion

During ion trap testing, RF signal with ~150 V amplitude is transmitted from interposer to the RF electrodes through TSVs, which will be a major challenge for dielectric liner (SiO2) of

TSVs. To assess the reliability of the TSV liner, a leakage current test is conducted. As illustrated in Fig. 4 (a), a standard TSV array for TSVs leakage current test is designed within the top die [11]. Since the routing interconnects of TSV array on the back side is not completed at the time of this writing, leakage current measurement on single TSV is carried out with this structure.

To evaluate the leakage property of TSV array, leakage current for RF electrodes in various ion trap configurations (Fig. 4 (b-d)) are measured and compared. As shown in Fig. 6, for RF electrodes in V80_TSV (10 TSVs) and REV_V40_TSV (12 TSVs), the leakage currents are 6 × 10-11 and 9 × 10-11 A, respectively, at 200 V. The total leakage current can be anticipated to correlate linearly with the number of parallel-connected TSVs. The high RF electrode leakage current of V40_TSV (20 TSVs accommodated) may be attributed to the much larger surface area of V40_TSV. However, if the peak voltage is set as 150 V, all the leakage currents show a significant decline as shown in Fig. 6.

Capacitance Measurement and Discussion

As capacitance is a key factor that determines the RF performance of ion trap, the capacitance value of traps with varying size is investigated. In addition, for TSV traps, the TSV induced capacitance should also be considered. Therefore, CV measurement is conducted on TSV traps and planar traps. To simplify the analytic model, similarly, the single metal oxide semiconductor (MOS) capacitance between surface electrode (RF) and grounding is firstly extracted and measured on the same test vehicles used in IV measurement (Fig. 7 (a)). The CV measurement was conducted with a voltage sweep from -30 to 30 V at AC frequency of 100 kHz. The capacitance curves for both planar TSV traps are plotted in Fig. 8.

The capacitance of TSV traps consists of two components, planar surface and TSVs. These two capacitors are in parallel as illustrated in the schematic (Fig. 7(b)). In the accumulation regime, oxide capacitance will dominate for both components. For planar capacitor, the capacitance per area (C_(planar_ox)) can be calculated using equation (1):

$$〖C〗_{(planar\_ox)}=\varepsilon_{ox}/t_{ox} \quad (1)$$

where ε_ox is the dielectric constant and t_ox (3 μm) is the thickness of oxide layer. For TSV capacitor, the capacitance for each TSV (C_(TSV_ox)) is expressed in equation (2) given by [14]:

$$C_{(TSV\_ox)}=(2\pi\varepsilon_{ox} l_{TSV})/(\ln(R_{ox}/R_{copper})) \quad (2)$$

where l_TSV (100 μm) is the length of TSV, R_ox (10.75 μm) is the radius of TSV trench (as etched) and R_copper (10 μm) is the radius of copper core.

When the gate voltage exhibits high negative values (for n-type substrate), a depletion layer will be formed in two spots, under the planar oxide layer and around TSV oxide liner. Thus, the capacitance of depletion layers will come into effect. Under this circumstance, the model should be modified where depletion layer capacitance is added in series with the original oxide capacitance as shown in Fig. 7(c). In the depletion regime, the thickness of depletion layers w_dep is a key factor and it can be expressed in equation (3) given by [15]:

$$w_{dep}=\sqrt{((2\varepsilon_{Si} 2\phi_B)/(qN_d))} \quad (3)$$

where ε_Si is dielectric constant of silicon, ϕ_B is the bulk potential and N_d is donor concentration. To determine the value of N_d, a spreading resistance profile is carried out from the trap surface down to 110 μm depth of silicon substrate to cover the whole TSV length. It is found that the doping concentration is consistent along vertical direction with ~7 × 1013 cm-3 concentration.

The depletion layers thickness w_dep is calculated to be 2.92 µm, similar to the planar oxide layer thickness (3 µm) but four times of TSV dielectric liner thickness (0.75 µm). This indicates that during depletion, the total capacitance of TSV will be dominated by TSV's depletion layer capacitance and consequently be lowered by ~25%. Nevertheless, the total capacitance of planar MOS will be maintained as the capacitance of planar depletion layer is much higher, relative to the oxide capacitance itself. This explains C-V curve shapes obtained in Fig. 8.

According to the surface area and TSV number per RF electrode, the capacitance of different-size ion traps can be analytically calculated using formulas listed above. In conjunction to the measurement outcomes, the results are summarized in Table II. The calculated capacitance values show a good match with the measured values. From the compiled outcomes, it can be postulated that higher capacitance is obtained from samples with larger surface area and more TSVs.

To evaluate the uniformity of the fabrication, a series of C-V measurements are conducted on dies from across the entire wafer. As shown in Fig. 9, the capacitance deviation is rather small for all investigated trap designs. This reflects high consistency and repeatability of trap fabrication across the whole wafer.

From C-V measurement, it is observed that though TSVs can increase the capacitance, the elimination of surface electrode area will evidently decrease it. Therefore, the TSV traps can result in better RF performance compared to their planar counterparts. In the future design, a surface electrode with a smaller area and less TSVs will be preferred.

Conclusions

Co-integration of TSVs and SE ion trap has been explored. Numerical modeling suggests that the modification of surface electrode configuration has negligible effect on the trapping height and trapping depth. Leakage current measurement shows that TSVs can withstand at least 200 V voltage and maintain a leakage current of 7 × 10-12 A. With the use of TSVs, surface electrode area can be scaled down significantly due to the omission of wire bonding pads. Thus, the overall capacitance has been reduced though TSVs are added. A better RF performance is expected for SE traps integrated with TSV. The given model of TSVs and surface electrode capacitance serve as a guideline for the future improvement and developments of ion trap designs.

Acknowledgments

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Table I. Trap Geometry Specifications

Trap name	RF line length (μm)	RF line width (μm)	Electrode area (mm^2)	Area reduction
V40	1460	40	12.40	79%
REV_V40_TSV	1460	40	2.56	
V80	2920	80	53.56	90%
V80_TSV	2920	80	5.32	

Table II. Capacitance computation and measurement results

	V40_TSV	REV_V40_TSV	V80_TSV	V80
Surface area per RF electrode (μm^2)	1070300	330700	233600	4569600
TSV number per electrode	20	12	10	0
Computed capacitance (pF), accumulation regime	18.32	7.40	5.69	51.90
Measured capacitance (pF), accumulation regime	19.30	8.31	6.60	53.30
Computed capacitance (pF), depletion regime	12.15	4.58	3.46	43.20
Measured capacitance (pF), depletion regime	14.60	6.48	4.65	49.20

Fig. 1. 3D model and layout of TSV trap design, (a) planar trap (V40) and (b) TSV trap (REV_V40_TSV) stacked on an interposer die with TSV connections and (c) layouts for different-size TSV traps.

Fig. 2. Trapping height and trapping depth comparison (before and after configuration modification) for different-size ion traps.

Fig. 3. Scanning Electron Microscope (SEM) images of TSV opening (a) overall, (b) top, (c) middle and (d) bottom of TSV.

Fig. 4. Optical images of (a) single TSV, (b) V80_TSV, (c) REV_V40_TSV and (d) left corner of V40_TSV. Marked areas are the position of TSVs under test.

The test vehicles for TSV leakage current test are illustrated in Fig. 7 (a). A metal pad serving as grounding plane is placed directly under the chip. One prober is contacted on the surface of top die, while the other prober is contacted on the grounding pad. In this case, leakage current from TSVs can be directly measured. Applying a dual voltage sweep ranging from -200 to 200 V with 2 V step, the leakage current of a single TSV is plotted in Fig. 5. From the 8 repeated measurements, it is observed that single TSV exhibits a maximum leakage current at about 7 × 10-12 A. From the measurement results, it can be postulated that the dielectric liner of TSV is able to sustain voltage range of -200 to 200 V and the leakage current level agrees well with Farooq et al. and Mehta et al.[12, 13].

Fig. 5. Repetitive test results for leakage current of single TSV.

Fig. 6. Statistics summary for leakage current of different-size ion traps @ 150 and 200V.

Fig. 7. (a) Schematic of test vehicle, (b) circuit mode at accumulation regime of TSV traps and (c) circuit model at depletion regime of TSV traps.

Fig. 8. Typical C-V curves for planar and TSV traps.

Fig. 9. Statistics summary for capacitance measurement results.

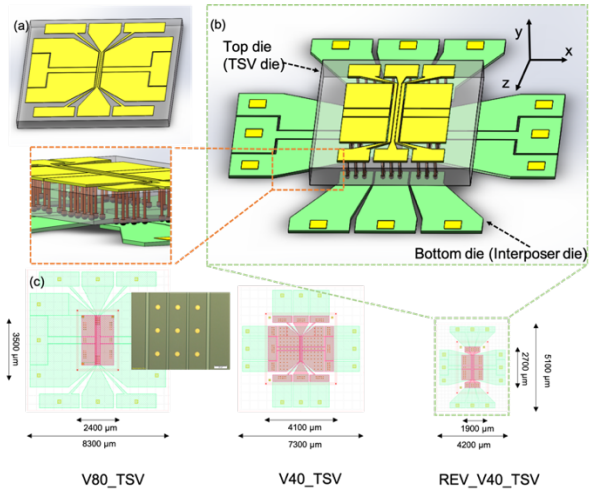

Fig. 1

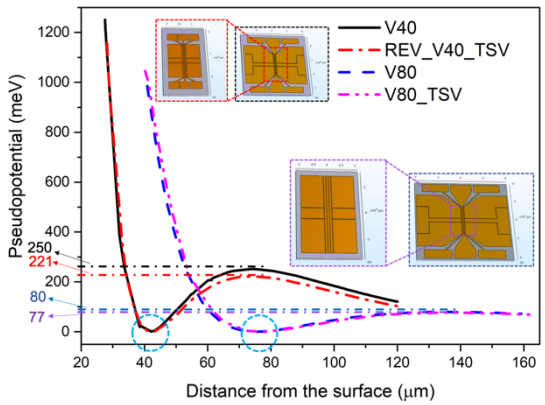

Fig. 2

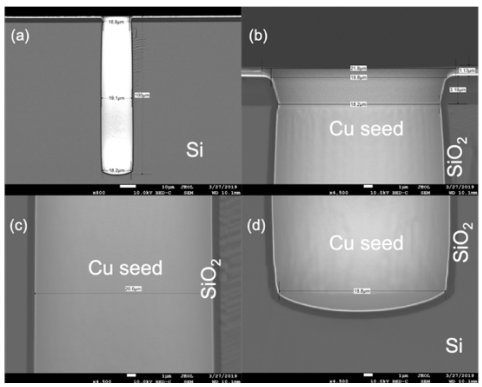

Fig3

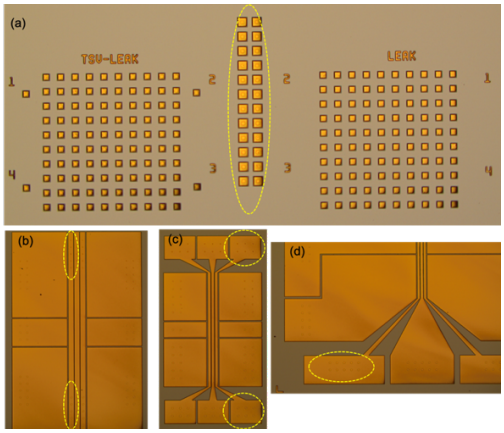

Fig. 4

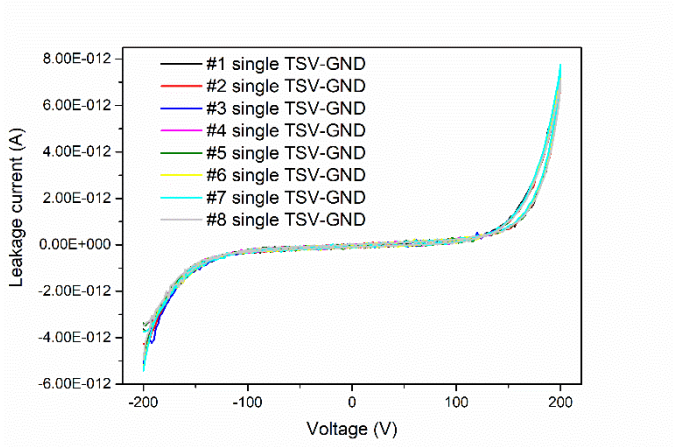

Fig. 5

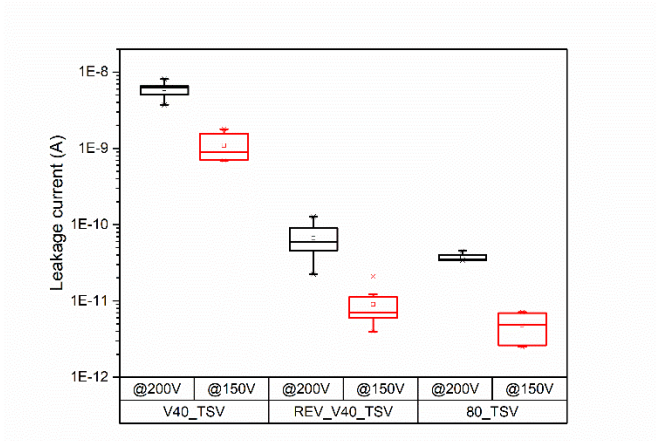

Fig. 6

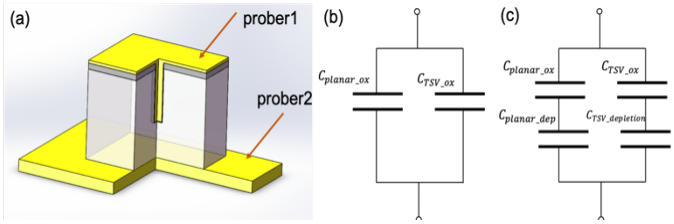

Fig. 7

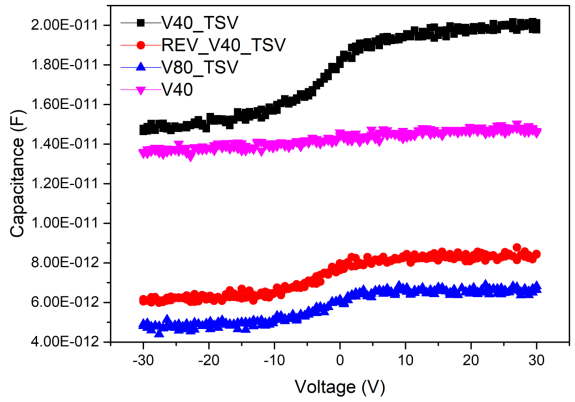

Fig. 8

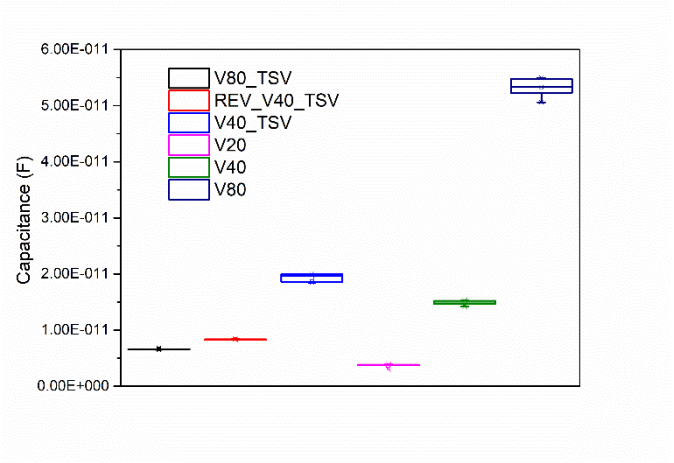

Fig. 9